Bias Sequencing and Gate Pulsing Circuit for GaN Amplifier

Apet Barsegyan, VinodhThangam, and Daniel Koyama

Integra Technologies, Inc., 321 Coral Circle, El Segundo, CA 90245, USA

abarsegyan@integratech.com

Abstract:

This article explores the design and performance of a bias sequencing and gate pulsing circuit used with a GaN HEMT power amplifier. With a focus on simple system integration, the circuit has been designed to enable the amplifier to operate from a single +50V supply.To make the amplifier fully autonomous, the gate pulsing circuit is designed to be triggered by RF input signal instead of conventional TTL external control.

Keywords:GaN, HEMT, Transistor, Amplifier, Bias Sequencing, Gate Pulsing

I INTRODUCTION

This paper describes a bias sequencing and gate pulsing circuit integrated onto a RF power amplifier assembly with Integra GaN transistor IGN1214M500 [1]. Measurements include pulse rise/fall time and delay, noise blanking. We briefly investigate bias temperature compensation as an option for enhancing performance.

II CIRCUIT REQUIREMENTS

Gallium Nitride (GaN) is becoming the power amplifier technology of choice for radar system designersseeking higher RF power densities, higher efficiency, and higher voltage operationcompared tolegacytransistor technologies such as silicon bipolar and Laterally Diffused MOS (LDMOS). In contrast to the more forgiving biasing requirements of enhancement-mode devices such as LDMOS, GaN has special bias sequencing requirements which system designers must accommodate to prevent damage to the devices.

1 Bias Sequencing

Depletion-mode devices such as GaNHigh Electron Mobility Transistors (HEMTs)require positive drain voltage with negative gate voltage to control the drain current. For safe operation, the negative gate voltage should be present before drain voltage is applied. During power-up, ideally one should pinch off the GaN device gate during the initial drain ramp-up. Likewise during power-down, the gate should be pinched off again as drain voltage is decreased to zero.

The circuit described in this paper accomplishes this bias sequencing function using a hot-swap controller IC [2] in combination with an N-Channel power MOSFET drain switch. The circuit contains a voltage regulator and voltage inverter to generate all internal voltages required by the sequencer, thereby enabling single supply operation.

2 Noise Blanking

For improved system performance, a noise blanking circuit was integrated with the bias sequencer. In radar systems, noise blanking improves receiver sensitivity by reducing the inter-pulse noise leakage in receive-mode during the pulse-off period. The noise blanking function is typically accomplished by switching the on/off bias of the power amplifier in sync with the RF pulse, where the off-state isolation of the amplifier provides the noise rejection during the off period. For this demonstration a gate pulsing approach was used, where the gate bias voltage is switched alternately between normal bias and pinch-off in sync with the RF pulse. Gate pulsing has the advantage of easier circuit implementation because of the low current and voltage switching requirement.

To facilitate system integration and demonstrate the concept of a simple "drop-in" amplifier solution, the gate pulsing circuit is designed to trigger from the RF input signal thereby eliminating the need for external system control. A detector/comparator circuit on the input side is used to sense the RF signal and activate the gate pulsing function. This gate pulsing approach has been used successfully for an Integra customer's LDMOS pallet amplifier operating at 2 ms pulse width and18% duty cycle.

All of the bias circuitry described above was incorporated onto the amplifier substrate assembly to make a "stand-alone" amplifier module (see figure 1).

Figure 1: IGN1214M500 Amplifier with bias sequencing and gate pulsing circuitry
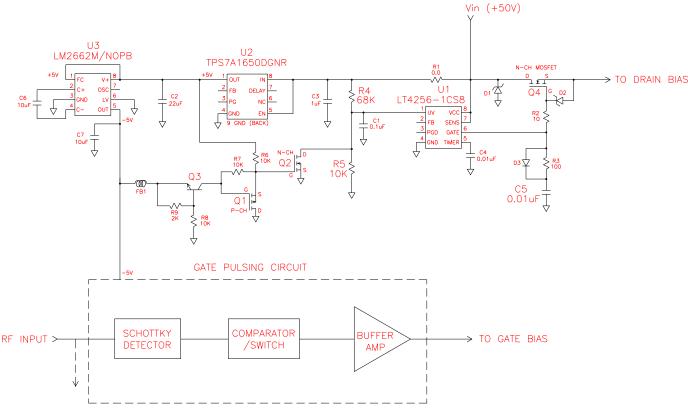
Figure 2: Schematic of Bias Sequencing and Gate Pulsing Circuit

III CIRCUIT DESCRIPTION

Referring to the schematic in figure 2, an N-channel power MOSFET Q4is used as a drain switch connecting the positive supply to the drain of the GaN device. Q4 has low Rds,on = 8.5 mΩ to minimize voltage drop, and up to 80A of current handling. Q4 is switched on and off via the GATE pin (pin 6) of controller U1.

At initial DC power-up, Q4 remains off while the +5V voltage regulator U2 and voltage inverter U3 turn on. The output of U2 drives the input of U3 to produce the -5V needed for the GaN transistor gate biasing. When the positive supply voltage reaches about +4 volts, U3 begins to turn on and negative voltage appears at its output. When U3 output voltage reaches about -4 volts, NPN transistor Q3 turns on, which turns on P-channel MOSFET Q1. With Q1 on, its source terminal goes to 0V, turning off N-channel MOSFET Q2. The open-circuit at the drain of Q2 disconnects it from the UV pin (pin1) of U1 and allows normal operation of the controller U1 to proceed. Whenever U3 is off or not fully on (i.e., is not outputting -4 volts or less), Q2 will be on, pulling the UV pin (pin 1) of the controller U1 down to 0V and forcing U1 to turn off Q4. This insures that no drain voltage is applied to the GaN device when the voltage inverter is not outputting at least -4 volts, and that the GaN device will always be pinched off initially when drain voltage is being applied to it.

As power-up proceeds, U1 becomes active and assumes control of the remaining bias sequencing process. When the UV pin (pin 1) of U1 reaches the low-to-high threshold voltage of 4V, the GATE pin (pin 6) of U1 begins to turn on

Q4, allowing drain voltage to be applied to the GaN device. The supply voltage at which this occurs can be set by resistors R4 and R5. As an example, for R4=68KΩ and R5=10KΩ, the supply voltage will begin to turn the drain on when it reaches 31V (31*10K/[10K+68K] = 4). The GATE pin (pin 6) of U1 utilizes a charge pump to provide a linear ramp-up of the drain voltage. This ramp-up time can be adjusted with capacitor C5.

For power-down, the process occurs in reverse except that the threshold level is slightly offset due to built-in hysteresis in controller U1 (high-to-low threshold, pin UV = 3.6V).For the example given above, the high-to-low threshold will be triggered when the supply voltage crosses 28V (28*10K/[10K+68K]=3.6) at which time Q4 turns off. As described earlier, the negative voltage will not begin to shut down until the supply voltage has dropped below about +4V.

The gate pulsing circuit is DC-poweredfrom the -5V output of the voltage inverter U3, but otherwise operates separately from the bias sequencer. In the off period of the RF pulse, the gate pulsing circuit is inactive and passes the -5V to the gate of the GaN transistor keeping it pinched off. In the pulse-on period, a Schottky diode detector circuit triggers a comparator/switch circuit which switches the gate voltage to the desired operating bias level. The bias can be set in a voltage divider circuit formed by an adjustable potentiometer. For fast switching time, a high-speed rail-to-rail op-amp was used in the buffer amplifier. Also, capacitance on the gate bias line following the switch was minimized to maintain fast rise/fall time.

The supply current draw of the sequencer/gate pulsing circuit is 17 mA @ +50V supply.

IV AMPLIFIER MEASUREMENTS

An Integra IGN1214M500GaN HEMT amplifier with on-board bias sequencing and gate pulsing circuitry was assembled and tested. The amplifier has typical output power of 500W and 13.5 dB RF gain at 60% efficiency over the 1.2 GHz to 1.4 GHz band.

The gate pulsing voltage waveform is shown in figure 3.The RF output pulse waveforms are shown in figure 4. Measured rise/fall times are 100 nanoseconds and 16 nanoseconds respectively. For comparison, the same transistor was tested in a fixture with normal gate biasing (no gate pulsing); the RF pulse waveforms are shown below in figure 5. With normal gate bias the rise time is 59 nanoseconds, and fall time is 15 nanoseconds.

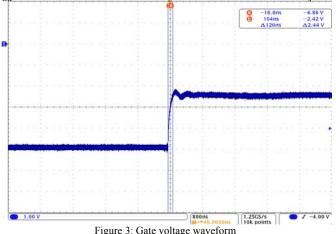Figure 6 showsdelay of the output pulse of approximately 10 nanoseconds relative to the input pulse.
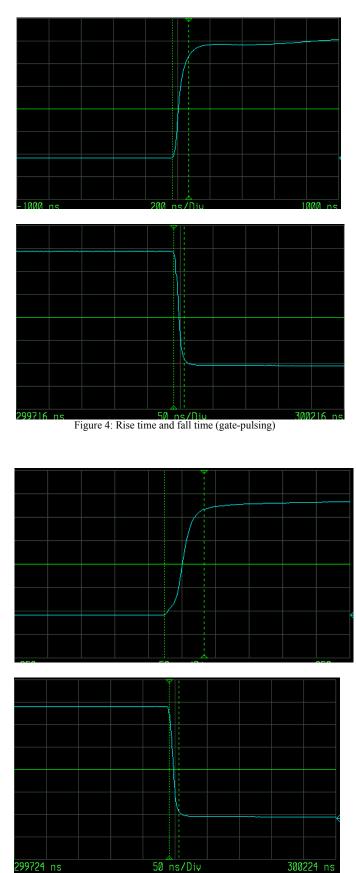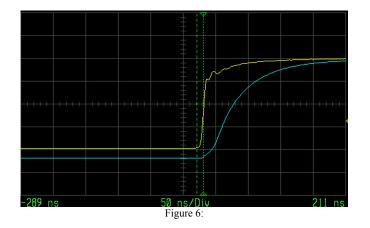

Figure 4: Rise time and fall time (gate-pulsing)

Figure 3: Gate voltage waveform

Figure 5: Rise time and fall time (normal gate bias)

Figure 6:

Figure 8: Idq vs. temperature

Frequency (GHz)	Input Noise (dBm/Hz)	Output Noise Normal Gate Bias (dBm/Hz)	Output Noise Gate Pulsing (dBm/Hz)
1.2	-126	-113	-147
1.3	-126	-113	-147
1.4	-126	-113	-148

Table 1: Amplifier noise power: normal gate bias vs. gate pulsing

Amplifier noise power was measured for normal gate bias (Idq=200 mA) and compared to measurements taken with gate pulsing. Results are shown in table 1. An improvement of about 34dB in noise rejection is achieved with gate pulsing.

VTEMPERATURE COMPENSATION

To achieve more consistent system performance over temperature, a temperature compensation circuit can be added to maintain a constant drain quiescent current. A typical implementation is shown in figure 7, wherethe temperature-dependent base-emitter voltage of PNP transistor MMBT2907 is used to generate the compensating voltage. Figure 8 shows Idq vs. temperature and figure 9 shows gate voltage vs. temperature (for constant Idq) for Integra GaN transistor IGN1214M500.Approximately+0.6 mV/°Cgate voltage compensationis required for this transistor.
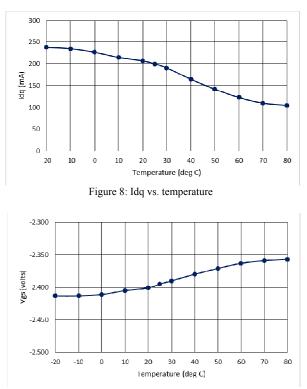

Figure 9: Vgs vs. temperature (constant Idq)

VICONCLUSION

An on-board bias sequencing and gate pulsing circuit has been designed and demonstrated on a power amplifier using IntegraGaN HEMT transistor IGN1214M500. With gate pulsing, rise time of 100 nS and fall time of 16nS was measured. Approximately 34dB improvement in noise rejection was measured with the gate pulsing circuit. To improve system performance over temperature, a simple temperature compensation circuit can be added to maintain constant bias for Integra GaN HEMT transistors with typically +0.6 mV/°C of compensation slope.

REFERENCES

[1] Integra datasheet IGN1214M500, www.integratech.com
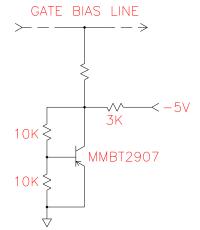[2] Linear Technology datasheet, www.linear.com/product/LT4256-1

Figure 7: Temperature Compensation circuit

BIO DATA OF AUTHORS

VinodhThangam received his B.S. in Electronics and Instrumentation from St. Peter's Engineering College in Chennai, India, and his M.S. in Electrical Engineering from the University of Arkansas. He joined Integra Technologies, Inc. in 2006 as an RF design engineer and has been involved in developing high performance RF power transistors and power amplifier modules for radar and avionics systems.

Apet Barsegyan is Vice President and Chief Operating Officer at Integra Technologies, Inc. A founding employee of Integra in 1997,hecurrently serves as an executive in technology development, sales, and operations management for the company. He received his Diploma Degree in Microwave Radiophysics from Yerevan State University, Armenia, and his MSEE in Microwave Engineering and Antennas from California State University, Northridge.

Daniel Koyama has been an RF engineer at Integra since 2013, supporting RF transistor and amplifier pallet design. Previously he has worked at Boeing and Raytheon, designing microwave circuits and modules for space and airborne radar applications. He received his B.S. inElectrical Engineering from UCLA.